

Set:

☐ Base  
☒ Display dimensions

Language:

S and ((upper or top) adj (electrode or plate)) and ((lower or bottom) adj (electrode or plate));

U	I	PT	P	Document ID	Issue Date	Pages	Title	Current OR	Current X
1				US 6335628 E2	20041228	18	Integrated circuit with a MOS capacitor	438/309	438/325;
2				US 6325129 E2	20041130	11	Method for manufacturing memory device	438/763	438/387;
3				US 6512042 E2	20041102	14	Capacitor and method for fabricating ferroelectric memory device with the same	439/3	438/637;
4				US RE38565 E	20040817	21	Thin film ferroelectric capacitors having improved memory retention through the use of essentially smooth bottom electrode structures	438/3	257/295;
5				US 6731494 E2	20030504	37	Capacitor and method for fabricating the same and semiconductor device	362/306.1	361/311;
6				US 6577230 E2	20040113	35	Method of manufacturing semiconductor device	439/620	361/329;
7				US 6574136 E1	20040106	38	Semiconductor device having driver circuit and pixel section provided over same substrate	257/408	257/295;
8				US 6642539 E2	20031104	16	Epitaxial template and barrier for the integration of functional thin film metal oxide heterostructures on silicon	257/43	257/344;
9				US 6461957 E1	20021008	35	Method of manufacturing semiconductor device	439/622	257/289;
10				US 6449754 E2	20030827	21	Thin film ferroelectric capacitors having improved memory retention through the use of essentially smooth bottom electrode structures	438/3	257/613;
11				US 6420172 E1	20020716	9	Method for removal of hard mask used to define noble metal electrode	438/702	257/295;
12				US 6380581 E1	20020430	23	DRAM technology compatible non volatile memory cells with capacitors connected to the gates of the transistors	257/314	216/161;
13				US 6281023	20010828	27	Completely encapsulated top electrode of a ferroelectric capacitor using a	438/3	216/39;